

TITLE OF THE INVENTION

SEMICONDUCTOR ELEMENT AND LIQUID CRYSTAL DISPLAY  
DEVICE USING THE SAME

BACKGROUND OF THE INVENTION

5 The present invention relates to a liquid crystal display device of an active matrix type used for displaying image data and character data from OA equipment or the like, and to the structure of an n-channel thin-film transistor used for this device.

10 A thin-film transistor (hereinafter abbreviated as TFT) has heretofore been used for driving liquid crystals of a pixel in a panel of a liquid crystal display device of the directly-viewing type. A simple switching element  
15 suffices for the performance of the TFT and, hence, amorphous silicon has been used as a semiconductor thin film. On the other hand, a liquid crystal display device of the projection type requires a high degree of brightness, and the TFT must be realized in a small size  
20 to increase the transmission factor. However, it was not allowed to decrease the size of the TFT formed by amorphous silicon since its current driving ability was so small. Therefore, so-called high-temperature polysilicon has been developed featuring an increased  
25 current driving ability by using quartz glass as a substrate and polycrystallizing amorphous silicon at a temperature as high as 900°C or higher.

30 However, quartz glass is very expensive and drives up the cost of production. Therefore, so-called low-temperature polysilicon has been developed by using an inexpensive glass substrate and polycrystallizing amorphous silicon by the irradiation with a laser beam.

35 In recent years, strikingly improved performance has been exhibited by the TFT formed by using the low-temperature polysilicon. Under such circumstances, it is

becoming a tendency to utilize the TFT not only as a switching element for driving the pixels of a panel in a liquid crystal display device but also for the peripheral drive circuits in the liquid crystal display device.

5 Moreover, a liquid crystal display device such as system-in-display is emerging being furnished with a memory function as well as various functions of CPU, interface, I/O and input by pen by using TFTs. In these cases, the role played by the TFT is not only limited to that of a  
10 simple switching element; i.e., performance and reliability are required by taking the logic circuits into account.

When the TFT is used as a logic element, eight kinds of voltage patterns will be applied to the three terminals of gate, source and drain as tabulated below, wherein "H" denotes a high level and "L" denotes a low level.

		Patterns							
		1	2	3	4	5	6	7	8
electrode	Gate	H	L	H	L	H	L	L	H
	Source	H	H	L	L	L	H	L	H
	Drain	L	L	H	H	L	H	L	H

20 So far, the TFT has been used for driving a liquid crystal pixel, and the above-mentioned patterns 1 to 4 have been exclusively used, i.e., relations of potential difference across the source and the drain have been exclusively used. When a potential difference develops  
25 across the source and the drain, a high electric field is established in the TFT, and a carrier having abnormally high energy (hereinafter referred to as hot carrier) is generated. The hot carrier that is injected into the gate oxide film causes a problem of deterioration in the  
30 characteristics of TFT.

It has heretofore been attempted to solve the

problem of hot carrier that generates when a high electric field is applied across the source and the drain. As a means for solving this problem, there have been proposed a lightly doped drain (LDD) structure and a 5 double drain structure as disclosed in "Submicron Device 2", by Mitsumasa Koyanagi, Maruzen Co., 1995, p. 187. According to these structures, a high electric field applied across the source and the drain is relaxed to prevent the generation of hot carrier. These structures 10 are with the case when a single crystal is used as a semiconductor. The same, however, also holds true even in the case of TFT.

#### SUMMARY OF THE INVENTION

15 However, there is almost no description concerning the problem of deterioration caused by a voltage application pattern 6 that is tabulated above. This is because, in the conventional TFT for simply driving the liquid crystal pixel, such a voltage application pattern 20 has seldom occurred. When a peripheral circuit is fabricated by using the TFTs, however, the voltage application pattern 6 tabulated above occurs in an analog switch used, for example, for a shift register.

In an n-channel TFT in which the source is assuming 25 "H" and the drain is assuming "H", in particular, the on-current drastically decreases and the TFT characteristics are deteriorated when a stress is applied to the gate, i.e., when "L" and "H" are alternatingly input to the 30 gate (hereinafter, this stress mode is referred to as gate-negative pulse mode). The cause of deteriorating the TFT characteristics in the gate-negative pulse mode is as described below. When the gate voltage changes from "H" into "L", the channel region changes from a 35 depletion layer in which no carrier is present into an accumulated layer in which holes are present in an excess

amount. In this case, holes are induced on the surface of the semiconductor thin film from the channel region of the semiconductor thin film. Here, it is considered that the holes gain high energy due to an electric field of a 5 gate-negative pulse and turn into hot holes which are then injected into the gate oxide film, whereby an interface level generates on the surface of the semiconductor device to greatly deteriorate the TFT characteristics.

10 The object of the present invention is to provide a TFT of a structure of which the characteristics are not deteriorated in the gate-negative pulse mode.

15 Moreover, the object of the present invention is to provide a liquid crystal display device which features a simplified circuitry and improved display quality by employing a TFT which is less deteriorated in the gate-negative pulse mode, for a liquid crystal display device of which the circuitry is becoming complex or of which the display quality is becoming poor due to limitation on 20 the range when utilizing the TFT which is deteriorated in the gate-negative pulse mode.

25 Furthermore, it is the object of the present invention to provide a liquid crystal display device equipped with a shift register having improved reliability by employing a TFT which is less deteriorated in the gate-negative pulse mode, for the shift register.

30 Moreover, it is the object of the present invention to provide a liquid crystal display device using an analog switch having improved reliability by utilizing a TFT which is less deteriorate in the gate-negative pulse mode, for the analog switch.

35 According to the present invention, the above-mentioned objects are accomplished by providing a semiconductor thin film of the TFT with a p-type semiconductor region that is in contact with a channel

region but is electrically connected to nowhere except the channel region. Upon employing this structure, holes induced on the surface by the gate-negative pulses are further supplied from the p-type semiconductor region.

5 The holes supplied from the p-type semiconductor region relax the electric field established by the gate-negative pulse. Therefore, the hot holes are less injected into the gate oxide film, and the TFT characteristics are less deteriorated. Besides, the p-type semiconductor region  
10 needs be connected to nowhere except the channel region and can, hence, be replaced by the conventional TFT, and an increase in the TFT area is confined to the p-type semiconductor region only.

According to the present invention, furthermore,  
15 the above-mentioned objects are accomplished by using the above-mentioned TFTs as the n-channel insulated gate thin-film transistors used for the liquid crystal display device, by using the above-mentioned TFTs as the n-channel insulated gate thin-film transistors to  
20 constitute shift registers in the peripheral circuit, and by using the above-mentioned TFTs as the n-channel insulated gate thin-film transistors to constitute analog switches in the peripheral circuit.

That is, the present invention is concerned with an  
25 n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising a semiconductor thin film formed on an insulating substrate and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are  
30 n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact  
35 with the channel region, and said p-type semiconductor

region is electrically connected to nowhere except the channel region.

The present invention is further concerned with an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising a gate electrode formed on an insulating substrate and a semiconductor thin film formed on said gate electrode via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just over the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with said channel region, and said p-type semiconductor region is electrically connected to nowhere except the channel region.

Moreover, the present invention is concerned with an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising an insulating film formed on a semiconductor substrate, a semiconductor thin film formed on said insulating layer and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with the channel region, and said p-type semiconductor region is electrically connected to nowhere except the channel region.

The present invention is further concerned with a liquid crystal display device comprising:

an active matrix including a plurality of scanning electrodes formed on an insulating substrate, a plurality

of video signal electrodes formed so as to intersect the scanning electrodes, thin-film transistors connected to the scanning electrodes and to the video signal electrodes, and pixel electrodes connected to said thin-film transistors;

5 a peripheral circuit formed on said insulating substrate by the same method as that of forming said thin-film transistors;

10 an opposing substrate opposed to said insulating substrate; and

liquid crystals held between said insulating substrate and said opposing substrate;

wherein said n-channel insulated gate thin-film transistors are used as said thin-film transistors.

15 In the liquid crystal display device, the TFT characteristics are little deteriorated when the above-mentioned n-channel insulated gate thin-film transistors are used for the shift registers in the peripheral circuit and, particularly, when the above-mentioned n-20 channel insulated gate thin-film transistors are used to play the role of analog switches in the shift registers in the peripheral circuit.

#### BRIEF DESCRIPTION OF THE DRAWINGS

25 Fig. 1 is a schematic plan view of a TFT according to the present invention;

Fig. 2 is a schematic sectional view along a line A-A' in Fig. 1;

30 Fig. 3 is a diagram illustrating the steps for producing the TFT according to the present invention;

Fig. 4 is a diagram comparing the degrees of degradation of when stress is applied to the TFT of the present invention and to the TFT of a conventional structure;

35 Fig. 5 is a schematic plan view illustrating a

bottom gate type TFT according to the present invention;

Fig. 6 is a schematic sectional view along a line A-A' in Fig. 5;

5 Fig. 7 is a schematic sectional view of an n-channel SOI-MOSFET according to the present invention;

Fig. 8 is a plan view of a unit pixel in a liquid crystal display device using the TFT of the present invention;

10 Fig. 9 is a plan view of an analog switch using the TFT of the present invention;

Fig. 10 is a diagram of a static shift register circuit using the TFTs of the present invention;

15 Fig. 11 is a block diagram of a peripheral circuit and an active matrix circuit in the liquid crystal display device constituted by using the TFTs of the present invention;

Fig. 12 is a schematic sectional view of a liquid crystal display device constituted by using the TFTs of the present invention;

20 Fig. 13 is a circuit diagram of a DA converter constituted by using the TFTs of the present invention; and

25 Fig. 14 is a circuit diagram of a static random access memory cell constituted by using the TFTs of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will now be described with reference to the drawings.

30 [Embodiment 1]

Fig. 1 is a schematic plan view illustrating a TFT according to the present invention, and Fig. 2 is a schematic sectional view along a line A-A' in Fig. 1. A substrate is a glass 100. A first layer is a thin polysilicon film 10. The thin polysilicon film 10 is

constituted by a source 11 and a drain 12 which are n-type semiconductor regions, a p-type semiconductor region 13, and a channel region 14 just under a gate 16 which is an intrinsic semiconductor region. A second layer is a 5 gate insulating film 15 which insulates the gate 16 and the thin polysilicon film 10 from each other. A third layer is the gate 16 having the same shape as the gate insulating film 15. Upon applying a positive voltage to the gate 16, an inverted layer in which the electrons are 10 present in an excess amount is formed in the channel region 14 to form a channel, whereby the source 11 and the drain 12 are rendered conductive to each other to obtain a switching operation.

In the TFT structure of this embodiment, the holes 15 induced on the surface due to a gate-negative pulse are further supplied from the p-type semiconductor region 13. The holes supplied from the p-type semiconductor region 13 relax the electric field established by the gate-negative pulse. Therefore, fewer hot holes are injected 20 into the gate insulating film 15, and the TFT characteristics are less deteriorated.

Fig. 3 illustrates the steps for producing the above-mentioned TFT. The sectional views of Fig. 3 correspond to a cross section along the line A-A' in Fig. 25 1. A thin amorphous silicon film is deposited maintaining a thickness of 60 nm on the glass substrate 100. Upon irradiating the thin film with a laser beam, amorphous silicon is polycrystallized to form a so-called low-temperature polysilicon. Depending upon the 30 photolithographic technology, furthermore, polysilicon is etched to form a thin polysilicon film 10 of the form of an island (Fig. 3(a)). Next, a silicon oxide 15a is grown in vapor phase to form a gate insulating film. Then, a metal 16a such as aluminum is deposited to form a 35 gate (Fig. 3(b)). Next, the gate and the gate insulating

film are etched relying upon the photolithographic technology to form a gate 16 and a gate insulating film 15 (Fig. 3(c)). Then, impurities of the Group 5 of periodic table, such as phosphorus ions, are implanted 5 into the thin polysilicon film by, for example, the ion-doping method to form n-type semiconductor regions that form a source 11 and a drain 12 (Fig. 3(d)). Then, impurities of the Group 3 of periodic table, such as boron ions, are implanted into the thin polysilicon film 10 by, for example, the ion-doping method to form a p-type semiconductor region (Fig. 3(e)). Thus, the TFT of the present invention is produced.

Fig. 4 illustrates the degrees of degradation of when pulse stress of "L" and "H" is applied to the gate 15 of the TFT of the present invention having the p-type semiconductor region 13 and to the gate of the conventional TFT without p-type semiconductor region with their source potential being maintained at "H" and drain potential being maintained at "H", and with "L" and "H" 20 pulse stress applied to the gate. The "L" level is set to be -15 V, the "H" level is set to be 0 V, and the pulse width is set to be 10  $\mu$ s. In Fig. 4, the ordinate represents the amount obtained by dividing an amount of change  $\Delta\mu$  in the mobility of TFT by an initial mobility 25  $\mu$ . When the life of the element is defined to be an amount of deterioration in the mobility  $\Delta\mu/\mu = 0.2$ , it will then be obvious from Fig. 4 that the TFT of the present invention exhibits a life extended into 50 times as long as that of the conventional TFT.

30 In this embodiment, the thin semiconductor film is formed of polysilicon. It, however, may be formed of amorphous silicon, single crystalline silicon, single crystalline germanium or the like.

Fig. 5 is a schematic plan view of a bottom' gate type TFT according to the present invention, and Fig. 6 is a schematic sectional view along a line A-A' in Fig. 5. A substrate is a glass 100. A first layer is a gate 16. 5 A second layer is a gate insulating film 15 which insulates the gate 16 and a thin polysilicon film 10 from each other. A third layer is the thin polysilicon film 10. In the thin polysilicon film 10 are formed a source 11 and a drain 12 which are n-type semiconductor regions, 10 a p-type semiconductor region 13, and a channel region 14 which is an intrinsic semiconductor region just over the gate electrode. A fourth layer is a channel protection film 50 for protecting the channel. Upon applying a positive voltage to the gate 16, an inverted layer in 15 which the electrons are present in an excess amount is formed in the channel region 14 thereby to form a channel, whereby the source 11 and the drain 12 are rendered conductive relative to each other to obtain a switching operation. In the TFT of this embodiment, when a 20 negative pulse is applied to the gate, holes are supplied into the channel region 14 from the p-type semiconductor region 13, and the TFT characteristics are prevented from being deteriorated.

25 [Embodiment 3]

Fig. 7 is a schematic sectional view of an SOI-MOSFET according to the present invention. Fig. 7 corresponds to Fig. 2 and Fig. 6, and in which are appearing a drain 12 and a p-type semiconductor region 13 30 in a semiconductor film 17. An insulating layer 19 is formed on a semiconductor substrate 18, and the semiconductor film 17 which is the first layer is formed on the insulating layer 19. The semiconductor film 17 is formed by, for example, single crystalline silicon or a 35 single crystal of gallium-arsenic. The semiconductor

film 17 is constituted by a source and a drain 12 which are n-type semiconductor regions, a p-type semiconductor region 13, and a channel region 14 which is an intrinsic semiconductor region just under the gate. A second layer 5 is a gate insulating film 15 which insulates the gate 16 and the semiconductor film 10 from each other. A third layer is the gate 16 having the same shape as the gate insulating film 15. Upon applying a positive voltage to the gate 16, an inverted layer in which the electrons are 10 present in an excess amount is formed in the channel region 14 thereby to form a channel, whereby the source and the drain 12 are rendered conductive relative to each other to obtain a switching operation. In the SOI-MOSFET structure of this embodiment, holes induced on the 15 surface due to a gate-negative pulse are further supplied from the p-type semiconductor region 13. The holes supplied from the p-type semiconductor region 13 relax the electric field established by the gate-negative pulse. Therefore, fewer hot holes are injected into the gate-insulating film 15, and the SOI-MOSFET characteristics 20 are less deteriorated.

[Embodiment 4]

Described below is an embodiment in which an active 25 matrix circuit and a peripheral circuit in the liquid crystal display device are fabricated by using n-channel FETs of the present invention.

Fig. 8 is a plan view illustrating a unit pixel in the liquid crystal display device constituted by using 30 the n-channel TFT of the present invention. A scanning electrode 22 and the gate of a TFT 20 of the present invention are connected together through a hole 21a, a signal electrode 23 and the drain of the TFT 20 of the present invention are connected together through a hole 21b, and a pixel electrode 24 and the source of the TFT 35

20 of the present invention are connected together through a hole 21c. The TFT 20 is turned on when a selection signal is input to the scanning electrode 22 and a voltage is applied to the gate of the TFT 20. A 5 video signal voltage is input to the signal electrode 23 while the TFT 20 is turned on, and is transmitted from the drain of the TFT 20 to the source thereof and is applied to the pixel electrode 24 to drive the liquid crystal. By using the TFT 20 of the present invention as 10 a pixel drive element, a drive waveform of a gate-negative pulse can be input to the pixel.

Fig. 9 is a plan view of an analog switch constituted by using the n-channel TFT of the present invention. This is a constitution in which the drain of 15 the n-channel TFT 20 of the present invention and the drain of the p-channel TFT 25 are connected together through a wiring electrode 26a to form Vin, the source of the n-channel TFT 20 of the present invention and the source of the p-channel TFT 25 are connected together 20 through a wiring electrode 26b to form Vout, and clocks having phases different by 180 degrees from each other are applied to the gate of the n-channel TFT 20 of the present invention and to the gate of the p-channel TFT 25. This is a switching circuit in which a signal input to 25 Vin is directly transmitted to Vout when the clock is assuming "H" and a signal input to Vin is interrupted when the clock is assuming "L". In this circuit, a gate-negative pulse mode is applied to the n-channel TFT 20 of the present invention when Vin and Vout are assuming "H". 30 Even in such a case, the n-channel TFT 20 of the present invention is not deteriorated unlike the conventional n-channel TFT, and a stable analog switch can be constituted.

Fig. 10 is a diagram illustrating one stage of a 35 static shift register circuit constituted by using the n-

channel TFTs of the present invention. One stage of the static shift register is constituted by four analog switches 61, 62, 63, 64, four inverters 65, 66, 67, 68, and power source lines  $V_{DD}$  and  $V_{SS}$  for supplying electric power to the inverters. One stage of the shift register works to delay a pulse wave input to  $V_{IN}$  by one clock and to send it to  $V_{OUT}$  and to the signal. The analog switches shown in Fig. 9 are used as the analog switches 61 to 64. In particular, a gate-negative pulse mode is frequently applied to the n-channel TFT 20 that constitutes the analog switch 62 in Fig. 10. Even in such a case, however, the n-channel TFT 20 of the present invention is not deteriorated unlike the conventional TFT, and a stable static shift register is realized.

Fig. 11 is a block diagram illustrating a liquid crystal display device constituted by using the n-channel TFTs of the present invention. A gate driver works to successively select the scanning electrodes connected to the gates of the unit pixel TFTs constituting the active matrix. The gate driver is constituted chiefly by the shift register. On the other hand, the source driver works to supply a signal voltage to the pixel electrodes that constitute the active matrix and the analog switch. By constituting the source driver and the gate driver by using at least the n-channel TFTs of the present invention, it is made possible to constitute a peripheral circuit and an active matrix circuit which are highly reliable.

Fig. 12 is a schematic sectional view of the liquid crystal display device of the present invention. Liquid crystals 27 are sandwiched between the lower glass substrate 100 including the active matrix circuit and an upper opposing glass substrate 200. Though not diagrammed,

scanning electrodes and signal electrodes 23 are formed like a matrix on the glass substrate 100 that includes the active matrix circuit, and a pixel electrode 24 is driven via an n-channel TFT 20 of the present invention 5 formed near an intersecting point thereof. Here, an interlayer insulating film 31 maintains the electric insulation between the pixel electrode and the TFT of the present invention and among the electrodes. On the opposing glass substrate 200 are formed a color filter 30 10 and a light-shielding film 29 that forms a black matrix pattern for shielding the light. The liquid crystals are in contact with an orientation film 28 so as to possess tilted angles.

Fig. 13 is a circuit diagram of a basic 6-bit DA 15 converter for converting a digital signal into an analog signal when a video signal is, for example, a digital signal. Six-bit digital signals D0 to D5 that are input are analyzed by a decoder, and the voltages are applied by the analog switches A0 to A63 to the resistors R0 to 20 R63 so as to be converted into analog voltage signals and are output to Vout. By using the TFTs of the present invention as the n-channel TFTs to constitute the analog switches A0 to A63, it is allowed to highly enhance the reliability of the analog switches.

Fig. 14 is a diagram illustrating a unit cell in a 25 static random access memory (SRAM) when the liquid crystal display device is equipped with, for example, a memory that is simply constituted by using n-channel TFTs and p-channel TFTs. The circuit itself is constituted in a customary manner. When a word line (WL) is selected to 30 assume the "H" level, the data of a bit line (BL) is stored in the SRAM. Here, by using the TFTs of the present invention as the n-channel TFTs, it is allowed to realize the SRAM having high reliability.

35 According to the present invention, the n-channel

TFT has the p-type semiconductor region which is in contact with the channel region. Therefore, the TFT is less deteriorated in the gate-negative pulse mode, and the reliability is improved. According to the TFT of the 5 present invention having the p-type semiconductor region in contact with the channel region, furthermore, the TFT is less deteriorated in the gate-negative pulse mode, making it possible to obtain a liquid crystal display device featuring improved reliability.

In Fig. 1:

- 13 -- p-type semiconductor region
- 14 -- channel portion (intrinsic semiconductor region)
- 10 -- thin polysilicon film
- 5 12 -- drain (n-type semiconductor region)
- 16 -- gate
- 11 -- source (n-type semiconductor region)

In Fig. 2:

- 10 16 -- gate 15 -- gate insulating film
- 12 -- drain 100 -- glass substrate
- 13 -- p-type semiconductor region

In Fig. 3:

- 15 10 -- thin polysilicon film 100 -- glass substrate
- 12 -- drain 13 -- p-type semiconductor region

In Fig. 4:

- 20 1 -- conventional TFT 2 -- TFT of the present invention
- 3 -- Number of pulses

In Fig. 5:

- 25 13 -- p-type semiconductor region
- 10 -- thin polysilicon film 12 -- drain
- 50 -- channel protection film 16 -- gate
- 14 -- channel region 11 -- source

In Fig. 6:

- 30 50 -- channel protection film
- 14 -- channel region 12 -- drain
- 17 -- semiconductor film 100 -- glass substrate
- 13 -- p-type semiconductor region 16 -- gate
- 15 -- gate insulating film

In Fig. 7:

- 16 -- gate 15 -- gate insulating film
- 17 -- semiconductor film 12 -- drain
- 19 -- insulating layer 18 -- semiconductor substrate
- 5 13 -- p-type semiconductor region

In Fig. 8:

- 23 -- signal electrode 20 -- TFT of the present invention
- 10 22 -- scanning electrode 21c -- through hole
- 24 -- pixel electrode

In Fig. 9:

- 25 -- p-channel type TFT
- 15 20 -- TFT of the present invention

In Fig. 10:

- 1 -- signal

In Fig. 11:

- 20 1 -- video signal 2 -- source driver
- 3 -- shift register X 4 -- analog switch
- 5 -- pixel TFT 6 -- liquid crystals
- 7 -- active matrix circuit 8 -- gate driver
- 9 -- shift register Y

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In Fig. 12:

- 20 -- TFT of the present invention

In Fig. 13:

- 30 1 -- reference potential